ABSTRACT OF THE DISCLOSURE

RESIDUE NUMBER SYSTEM ARITHMETIC CIRCUITS WITH BUILT-IN SELF TEST

An arithmetic circuit for use with an RNS is provided. The arithmetic circuit includes an arithmetic core, test circuitry, and logic circuitry. The arithmetic core performs an RNS arithmetic operation, and the test circuitry verifies proper circuit delay by inducing oscillation at the output of the arithmetic core during testing. The logic circuitry produces a pass/fail signal based on whether the oscillation frequency of the arithmetic core is at least equal to a minimum threshold value. In one preferred embodiment, the logic circuitry includes a counter that counts oscillations of the output of the arithmetic core during testing, and a comparator that compares the output of the counter after a predetermined test period with the minimum threshold value. Also provided is a method for testing the propagation delay of an RNS arithmetic circuit having an arithmetic core. According to the method, the output of the arithmetic core is fed back to one of the inputs of the arithmetic core, and a constant is provided to another input of the arithmetic core so as to induce oscillation at the output of the arithmetic core. A pass/fail signal is produced based on whether the oscillation frequency of the arithmetic core is at least equal to a minimum threshold value.

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